L7: Entry 2 of 9 File: USPT May 30, 2000

DOCUMENT-IDENTIFIER: US 6070205 A
TITLE: High-speed processor system having bus arbitration mechanism

Abstract Text (1):
A high-speed processor system having a bus arbitration mechanism constructed on a single semiconductor chip. The processor system comprises at least one bus master, a plurality of buses and a plurality of bus slaves. Each bus comprises an independent address bus, an independent data bus and individual data transfer capability. Every bus master comprises a plurality of independent bus interfaces each connected to one of the buses. Each bus slave is connected to a bus that has corresponding data transfer capability. For a system having more than two bus masters, the system further comprises a plurality of bus arbitrators for arbitrating the access of each bus independently. The bus arbitrator receives a bus request signal from each bus master that requests the bus access and issues a bus grant signal to the bus master allowed to access the bus. The bus arbitrator comprises a plurality of priority order information storage devices for storing priority order information for all the bus masters connected to the bus. At every bus cycle, one set of priority order information is selected continuously and cyclically. When more than one bus master requests the bus access at the same time, the bus arbitrator determines which bus master may access the bus according to selected priority order information.

Detailed Description Text (25):
FIGS. 5, 6 and 7 illustrate only a single bus arbitration mechanism. The high-speed processor system of this invention, however, may have more than one bus, each having its own bus arbitrator and data transfer capability. As an example, the system may comprise a first bus for handling data transfer and exchange between bus masters and faster bus slaves and a second bus for handling data transfer and exchange between bus masters and slower bus slaves. Under this circumstance, a first arbitrator and a second arbitrator will be arbitrating the first and second buses respectively.

Detailed Description Text (27):
FIG. 8 illustrates an embodiment of the overall high-speed processor system having bus arbitration mechanisms according to the present invention. In the embodiment, the processor system comprises first and second buses and a plurality of bus masters including a CPU 1301, a Picture Processor 1302, a Sound Processor 1303 and a DMA (Direct Memory Access) controller 1304, all connected to both buses. It also comprises a plurality of bus slaves including an internal memory 1305, an I/O control circuit 1308, a universal timer 1309, an A/D converter 1310 and an optional DRAM refresh controller 1315, all connected to the first bus. A first bus arbitrator 1306 and a second bus arbitrator 1307 provide the arbitration for first and second buses respectively. The processor system also include a PLL (Phase Locked Loop) circuit 1311, a clock driver 1312, a low voltage detector 1313 and an external memory interface 1314.

Detailed Description Text (37):
The I/O control circuit 1308 handles communication between the high-speed processor and external devices. The universal timer 1309 controls one of interrupt request signals to the CPU 1301 according to the time interval set by the application

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software. The A/D converter 1310 converts an analog voltage input signal into a digital signal.

Detailed Description Text (43):
In the high-speed processor system, the Picture Processor 1302, the Sound Processor 1303, the DMA controller 1304, the I/O control circuit 1308, the universal timer 1309, and the A/D converter 1310 are capable of issuing interrupt request signals to the CPU.

Detailed Description Text (109):
The size of the second bus arbitration circuit is much smaller than that of the first bus arbitration circuit in FIG. 14 because only eight sets of programmable information storage devices and fixed information storage devices are included. Although both the number of the fixed priority order information storage devices and that of the programmable priority order information storage devices are illustrated as eight, the number is not limited to eight. According to factors such as the number of bus masters, the required types of priority order, the size of the arbitration circuit and so on, the number can be designed to satisfy the requirement.